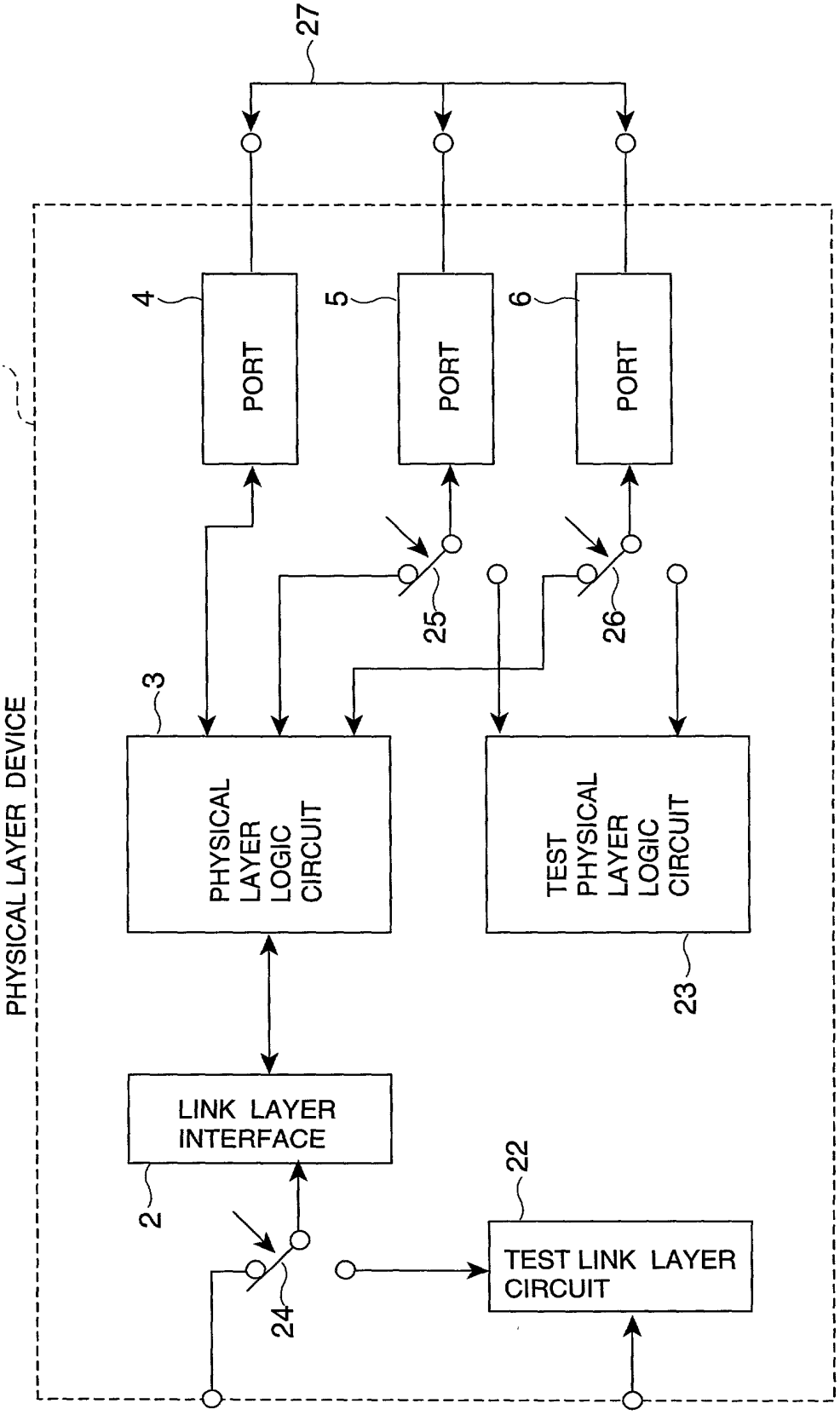

FIG. 1

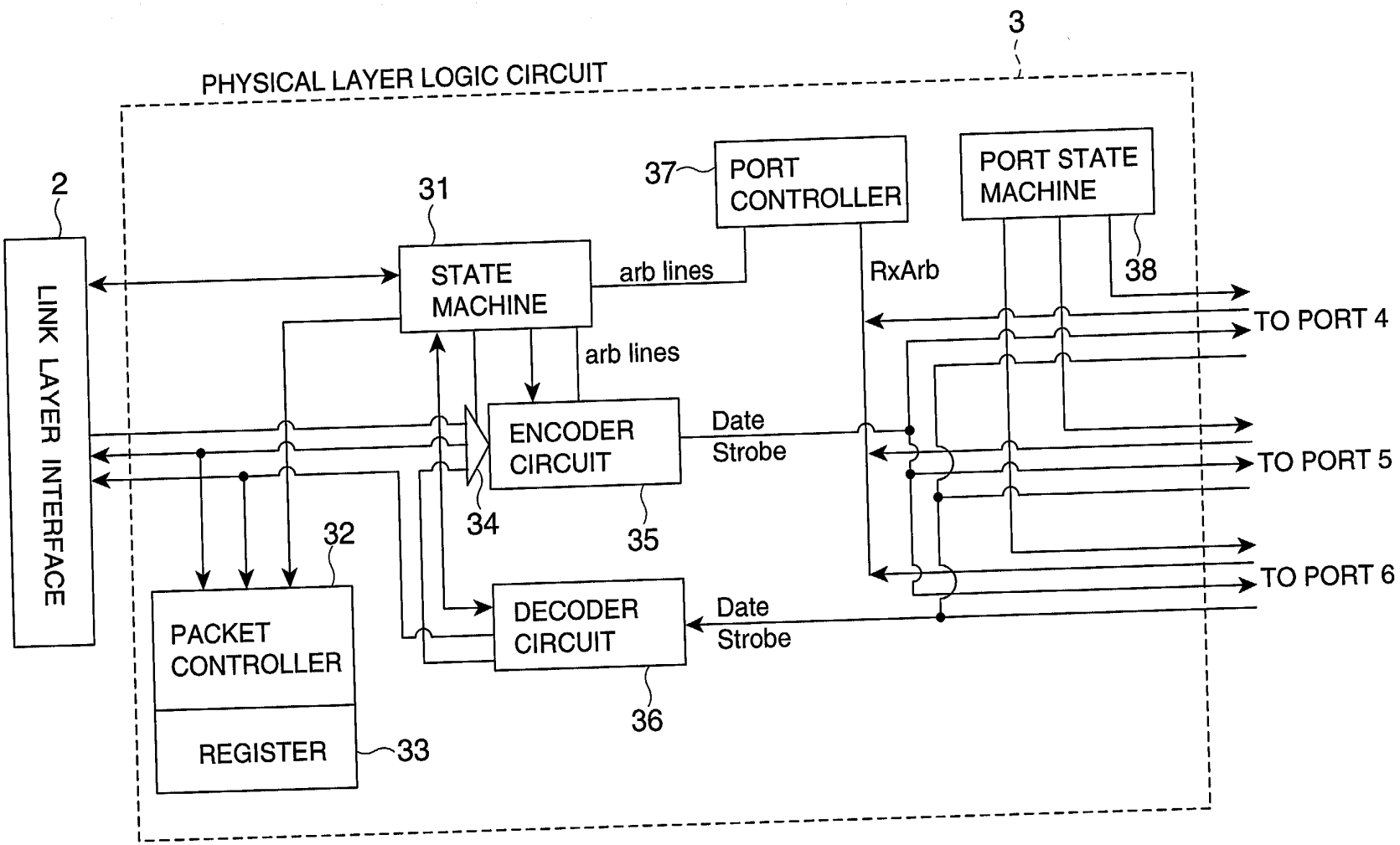

FIG. 2

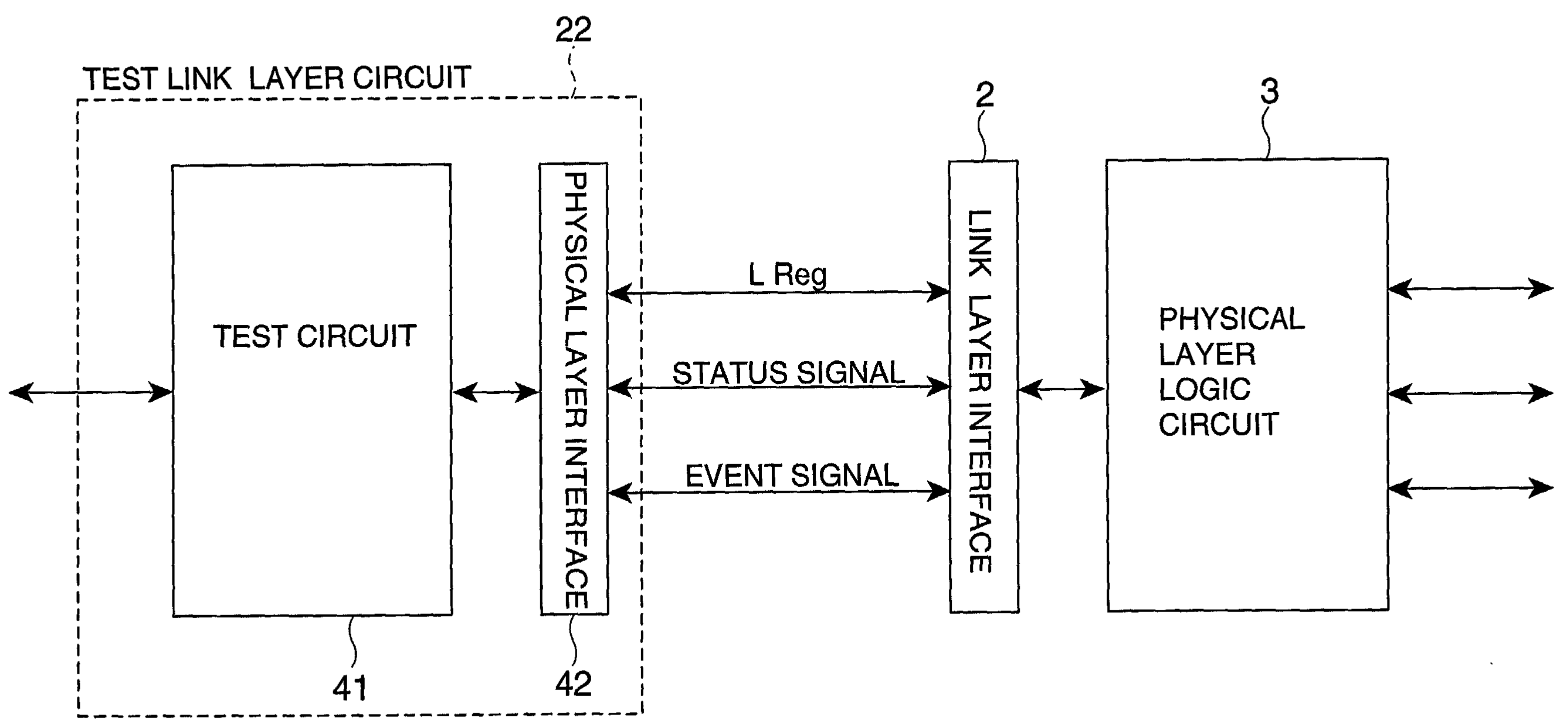

FIG. 3

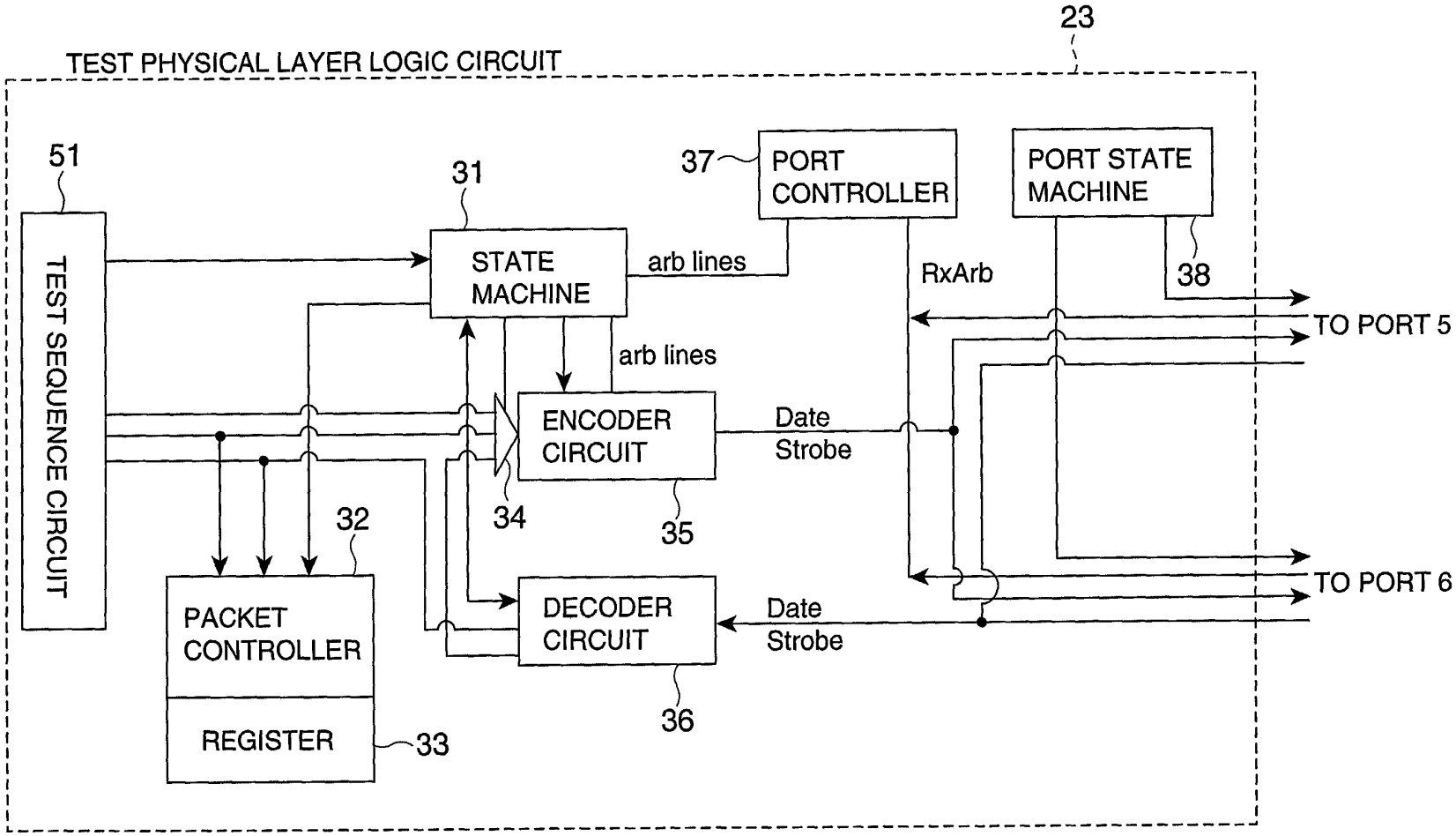

FIG. 4

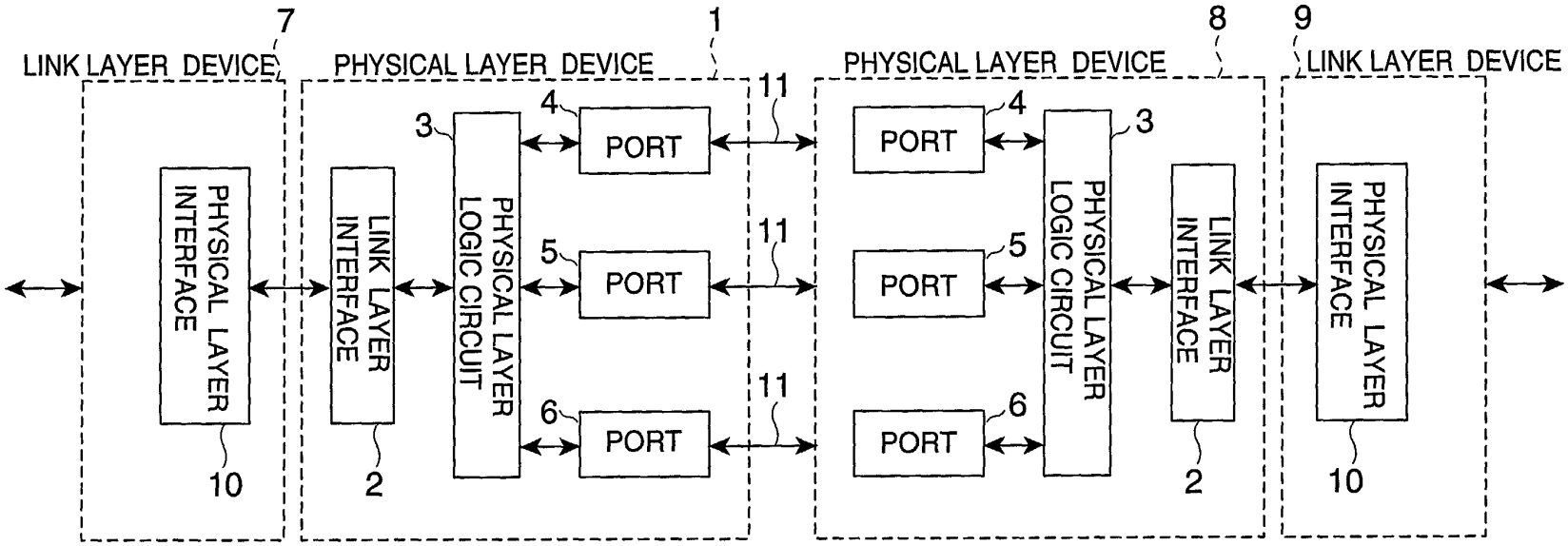

FIG. 5

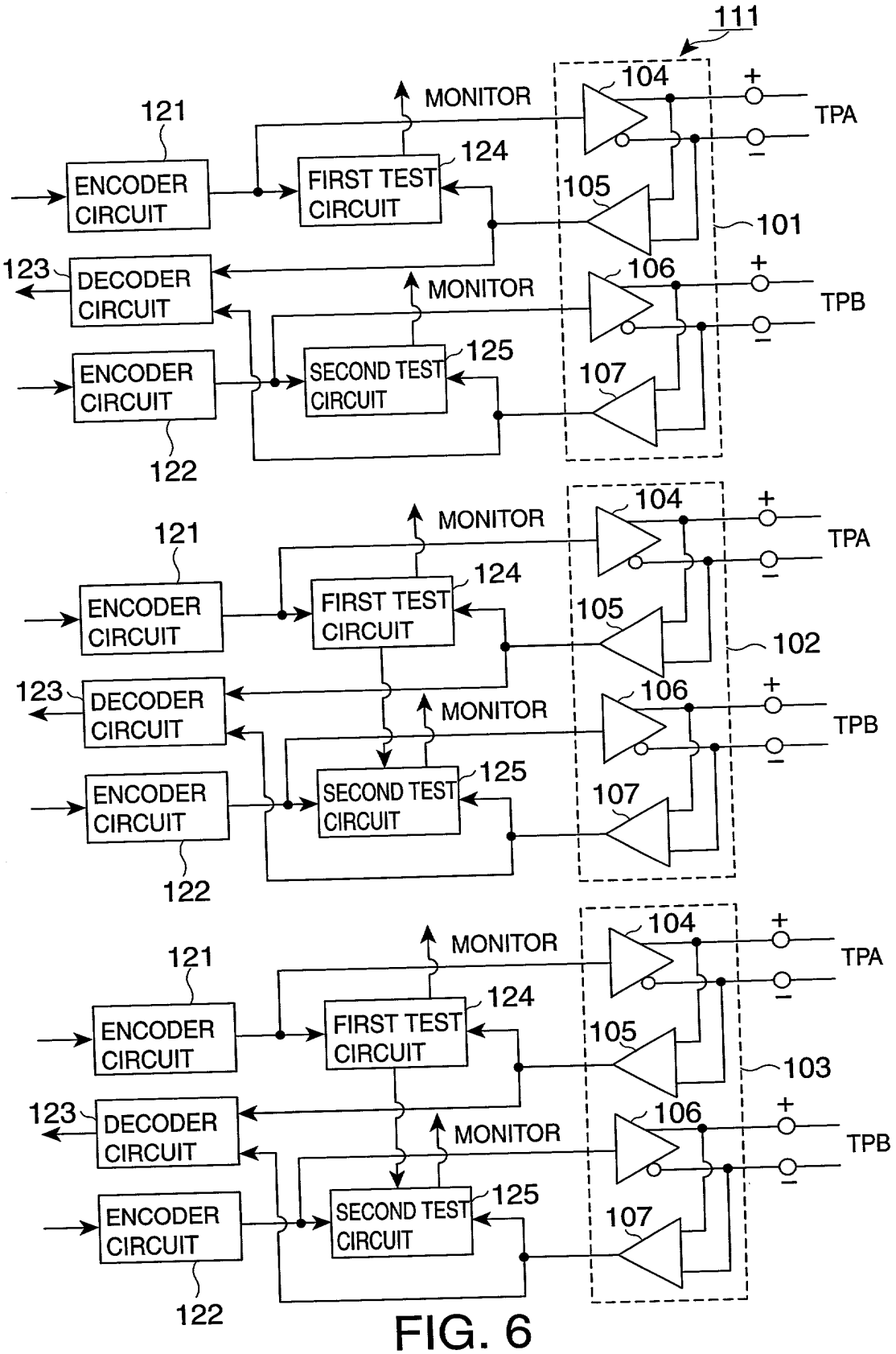
111
104
+
TPA
−
MONITOR
121
124
ENCODER CIRCUIT
FIRST TEST CIRCUIT
105
101
123
DECODER CIRCUIT
106
MONITOR
+
TPB
−
ENCODER CIRCUIT
SECOND TEST CIRCUIT
125
107
122
104
+
TPA
−
MONITOR
121
124
ENCODER CIRCUIT
FIRST TEST CIRCUIT
105
102
123
DECODER CIRCUIT
106
MONITOR
+
TPB
−
ENCODER CIRCUIT
SECOND TEST CIRCUIT
125
107
122
104
+
TPA
−
MONITOR
121
124
ENCODER CIRCUIT
FIRST TEST CIRCUIT
105
103
123
DECODER CIRCUIT
106
MONITOR
+
TPB
−
ENCODER CIRCUIT
SECOND TEST CIRCUIT
125
107
122

FIG. 6

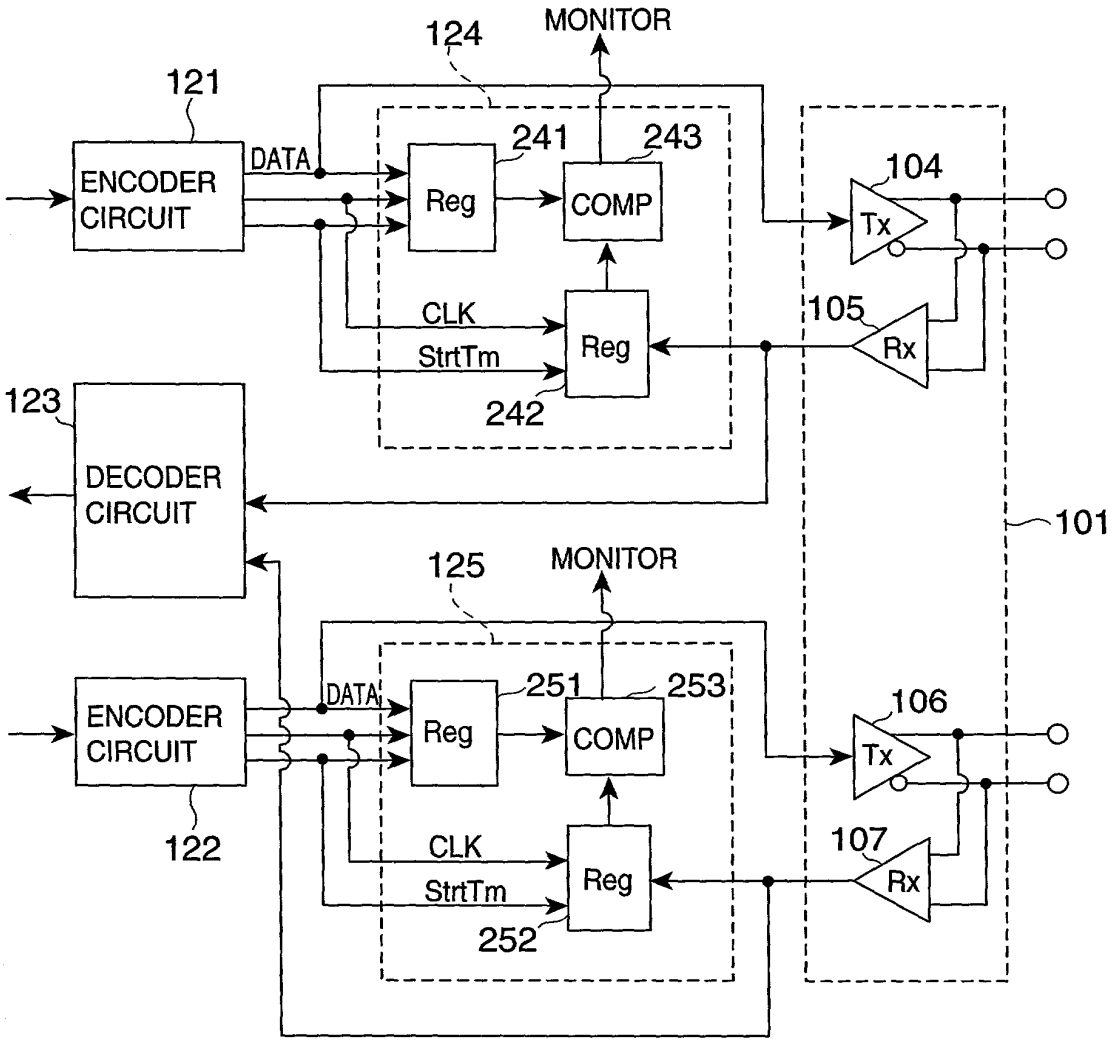
124
MONITOR
121
ENCODER CIRCUIT
DATA
241
243
Reg
COMP
104
Tx
CLK
StrtTm
Reg
105
Rx
242
123
DECODER CIRCUIT
101
125
MONITOR
ENCODER CIRCUIT
DATA
251
253
Reg
COMP
106
Tx
122
CLK
StrtTm
Reg
107
Rx
252

FIG. 7

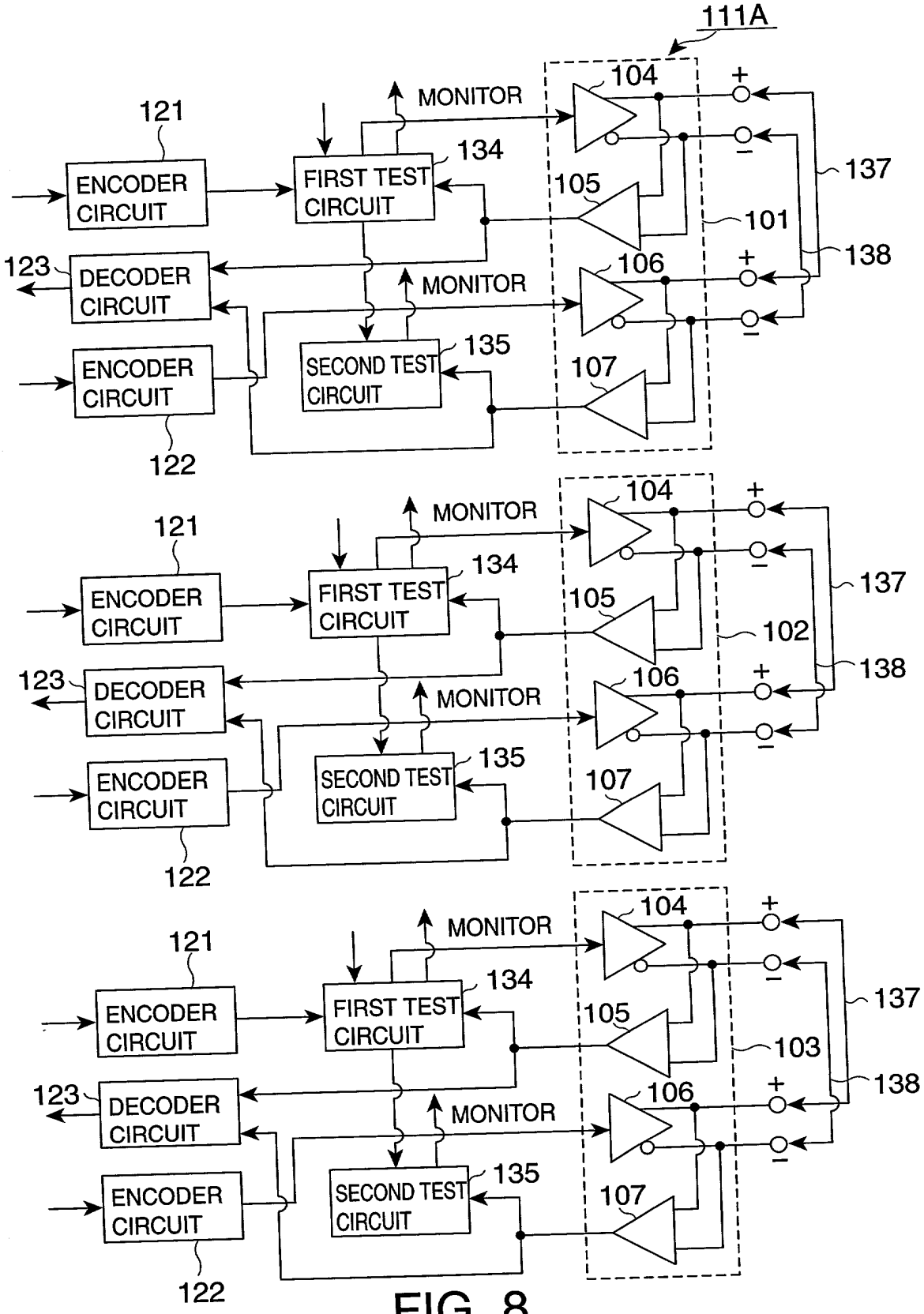
111A
121
ENCODER CIRCUIT
FIRST TEST CIRCUIT
134
MONITOR
104
105
101
137
138
123
DECODER CIRCUIT
106
MONITOR
ENCODER CIRCUIT
SECOND TEST CIRCUIT
135
107
122
102
103

FIG. 8

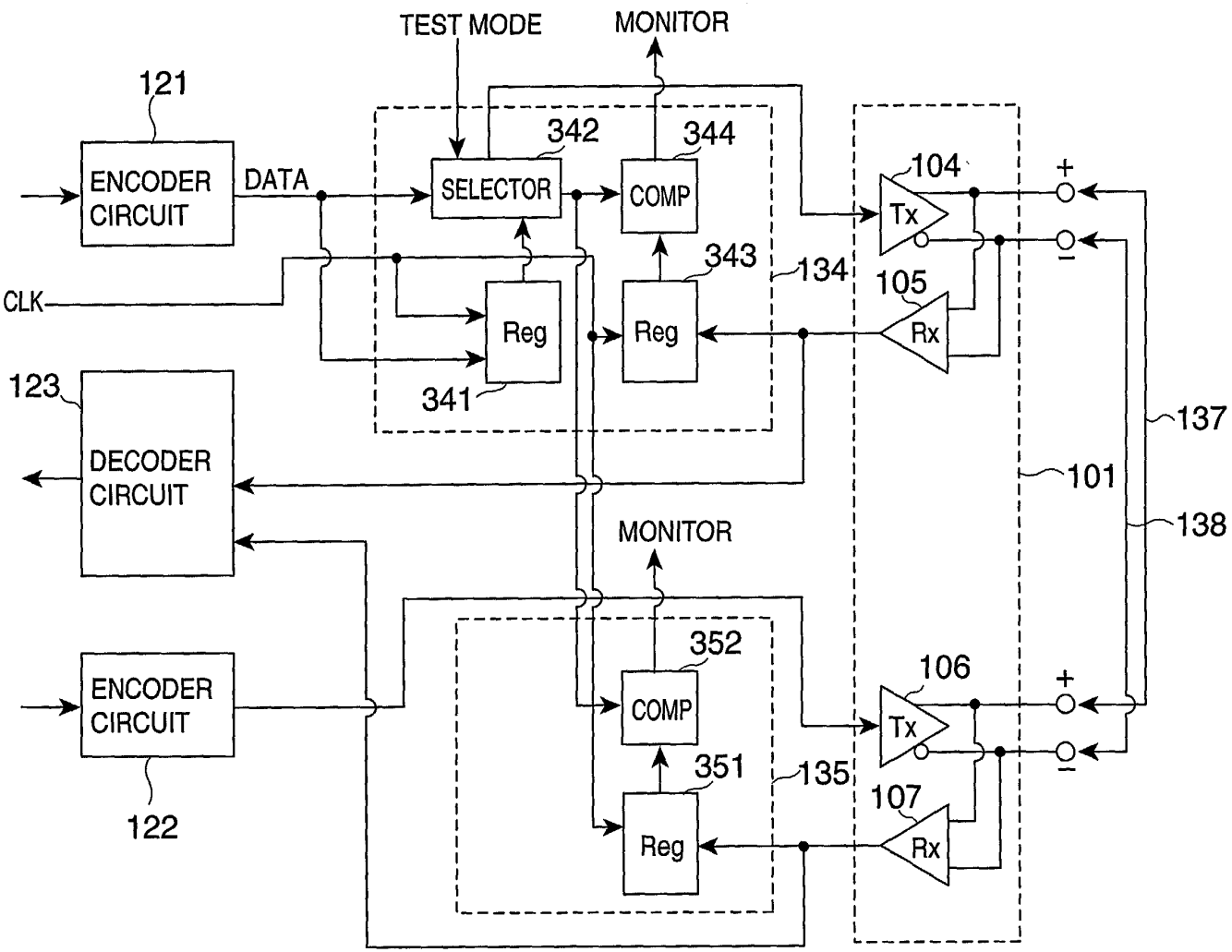

FIG. 9

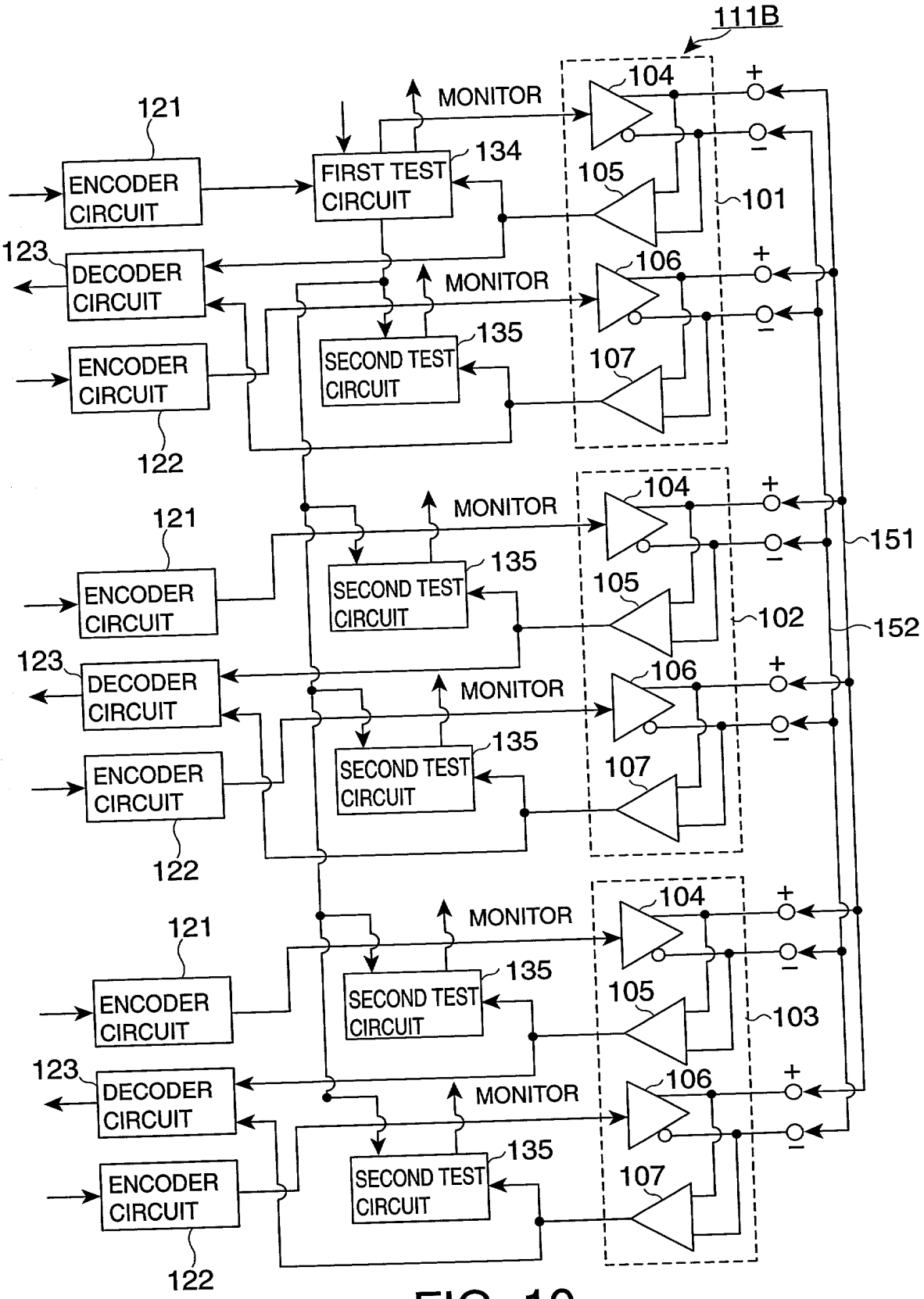
111B
104
MONITOR
+
121
ENCODER CIRCUIT
FIRST TEST CIRCUIT
134
105
101
123
DECODER CIRCUIT
106
MONITOR
135
SECOND TEST CIRCUIT
107
ENCODER CIRCUIT
122
151
102
152
103

FIG. 10

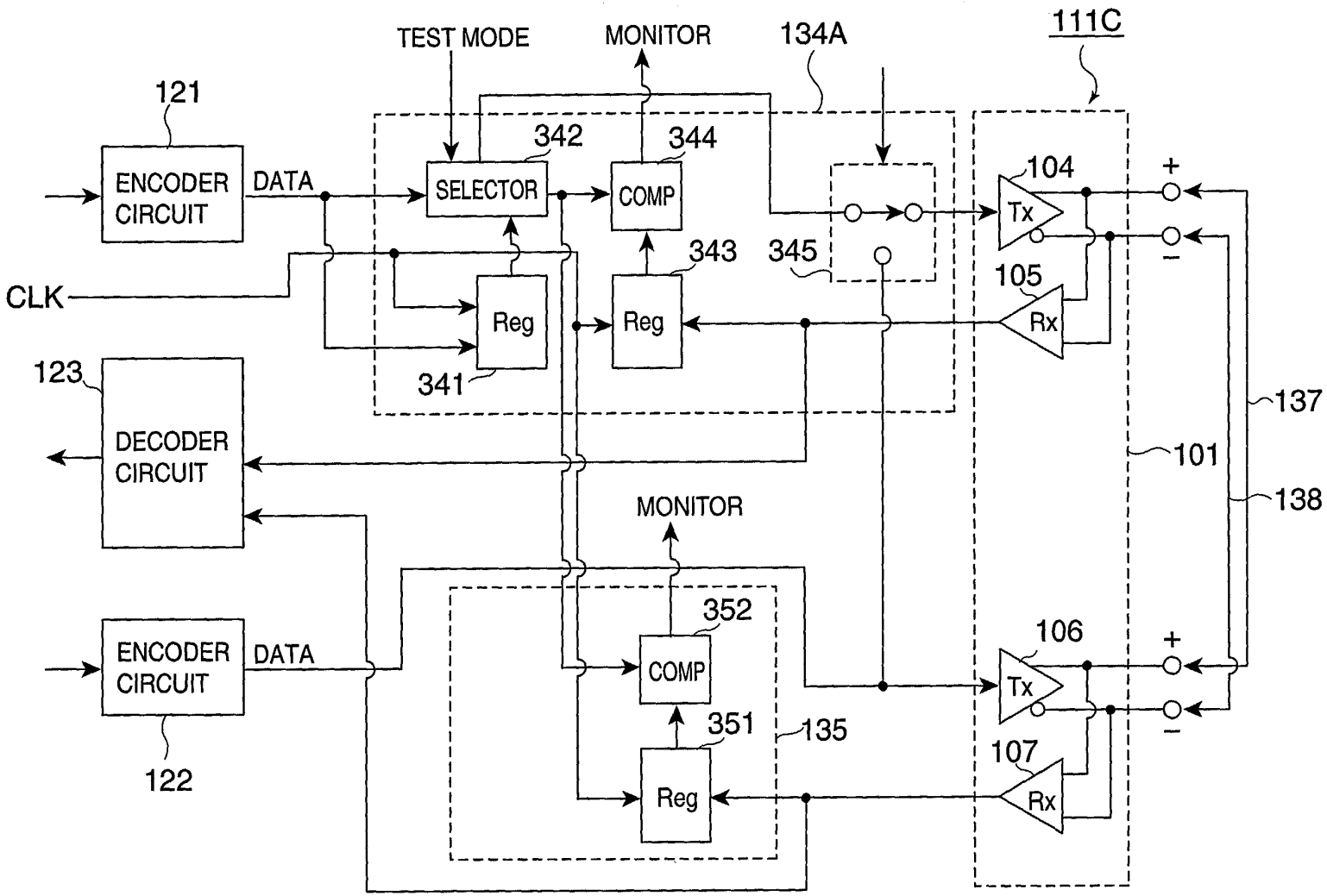

FIG. 11

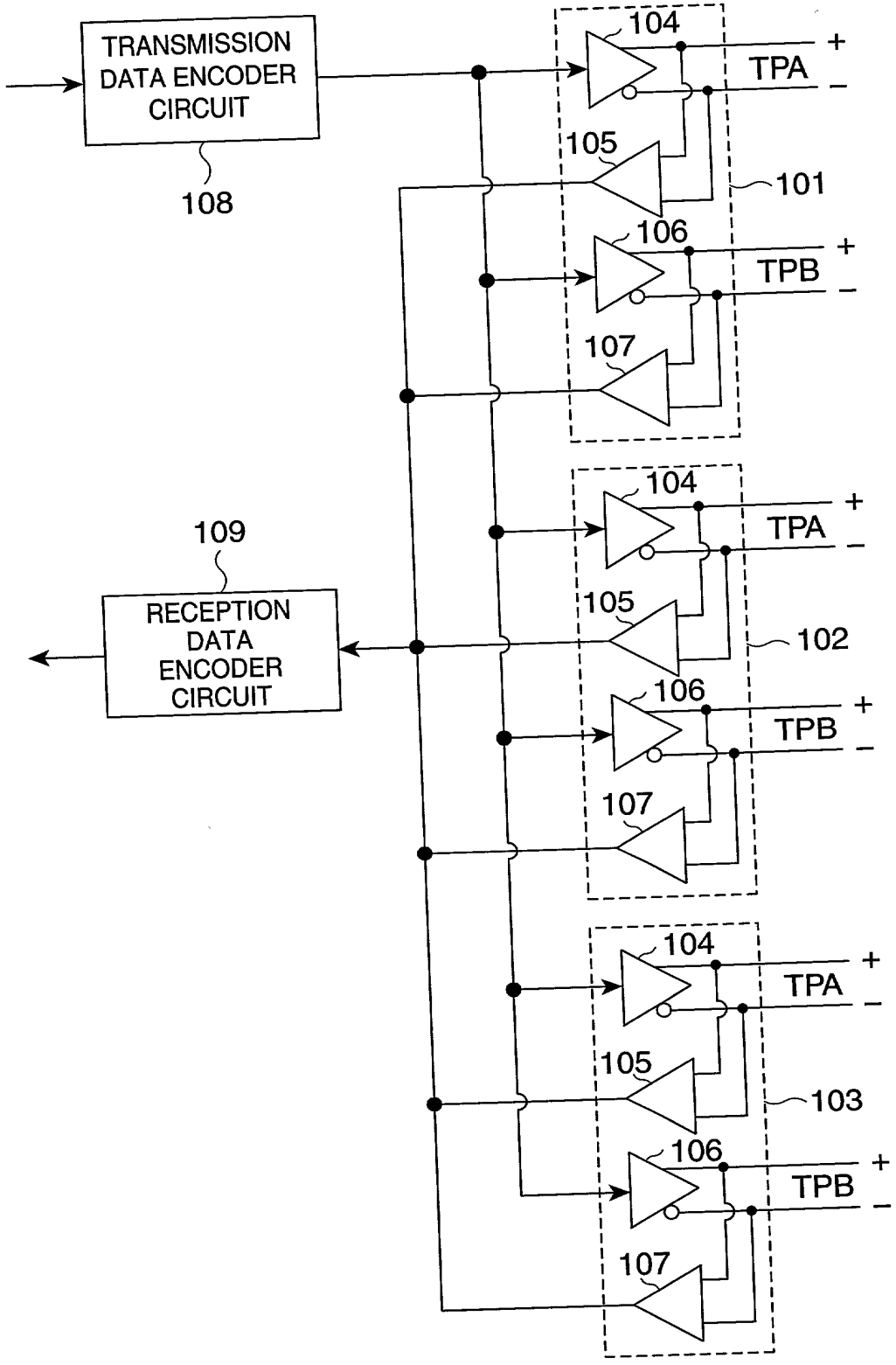
TRANSMISSION DATA ENCODER CIRCUIT
108
104
TPA
+
−
105
101
106
TPB
+
−
107
109
RECEPTION DATA ENCODER CIRCUIT
104
TPA
+
−
105
102
106
TPB
+
−
107
104
TPA
+
−
105
103
106
TPB
+
−
107

FIG. 12